In the Claims:

Claims **1 to 20** (canceled).

21. (previously presented) A method of testing an integrated circuit comprising the steps:

a) providing at least one output signal generated by a circuit unit of said integrated circuit to at least one signal output pin of said integrated circuit during a normal operating mode;

b) externally applying an externally applied potential to at least one selected output pin among said at least one signal output pin;

c) evaluating a potential value of said externally applied potential;

d) dependent on and responsive to a result of said evaluating, switching from said normal operating mode into a test mode; and

e) during said test mode, generating in said circuit unit at least one test signal that is to be tested, and proving said at least one test signal to at least one chosen output pin among said at least one signal output pin.

22. (previously presented) The method according to claim 21, wherein said step b) comprises connecting a passive circuit component to said at least one selected output pin and

generating said externally applied potential through said passive circuit component.

23. (previously presented) The method according to claim 22, wherein said step b) further comprises connecting said passive circuit component between said at least one selected output pin and a reference potential.

24. (previously presented) The method according to claim 22, wherein said passive circuit component comprises a resistor.

25. (previously presented) The method according to claim 21, wherein said at least one selected output pin in said step b) and said at least one chosen output pin in said step e) both comprise the same output pin among said at least one signal output pin.

26. (previously presented) The method according to claim 21, wherein said at least one signal output pin comprises plural signal output pins including a first output pin and a second output pin that is distinct and separate from said first output pin, said at least one selected output pin in said step b) is said first output pin, and said at least one chosen output pin in said step e) is said second output pin.

27. (previously presented) The method according to claim 21,

further comprising varying said externally applied potential so that said potential value of said externally applied potential is initially a first potential value and is then a second potential value different from said first potential value,

wherein said at least one test signal generated in said step e) comprises plural test signals including a first test signal and a second test signal different from said first test signal; and

further comprising providing said first test signal to said chosen output pin dependent on and responsive to said evaluating in said step c) determining that said externally applied potential has said first potential value, and providing said second test signal to said chosen output pin dependent on and responsive to said evaluating in said step c) determining that said externally applied potential has said second potential value.

28. (previously presented) The method according to claim 27, wherein said circuit unit comprises plural circuit blocks including a first circuit block and a second circuit block, and further comprising activating said first circuit block and deactivating said second circuit block dependent on and responsive to said evaluating in said step c) determining that said externally applied potential has said first potential value, and activating said second circuit block and deactivating said first circuit block dependent on and

responsive to said evaluating in said step c) determining that said externally applied potential has said second potential value.

29. (previously presented) The method according to claim 21, wherein said circuit unit comprises plural circuit blocks, and further comprising respectively activating and deactivating different ones of said circuit blocks dependent on and responsive to a result of said evaluating.

30. (previously presented) The method according to claim 21, wherein said steps d) and e) are carried out at a time separate from said steps b) and c), and not overlapping with said steps b) and c).

31. (previously presented) The method according to claim 21, wherein said evaluating in said step c) comprises comparing said potential value to at least one reference value.

32. (previously presented) The method according to claim 21, wherein said evaluating in said step c) comprises comparing said potential value to at least one reference value range defined by an upper reference value and a lower reference value, so as to determine whether said potential value falls in said reference value range.

33. (previously presented) The method according to claim 21, wherein said evaluating in said step c) comprises

performing a logical operation on said potential value and a signal value of said at least one output signal generated by said circuit unit.

34. (previously presented) The method according to claim 33, wherein said step d) switches into said test mode only when said signal value is zero and said potential value lies in a prescribed potential value range.

35. (previously presented) The method according to claim 21, wherein said evaluating in said step c) comprises determining whether said potential value lies within a voltage interval of a voltage window discriminator, and said step d) switches into said test mode only when said potential value does lie within said voltage interval of said voltage window discriminator.

36. (previously presented) The method according to claim 35, wherein a signal value of said at least one test signal also lies within said voltage interval of said voltage window discriminator.

[RESPONSE CONTINUES ON NEXT PAGE]

In the Drawings:

Please replace the original drawings (two sheets including Figs. 1 and 2) with the enclosed new Replacement Sheets of formal drawings (three sheets including Figs. 1, 2 and 3 thereon). The new Replacement Sheets incorporate the proposed drawing revisions that were submitted on June 17, 2003 and that have been approved by the Examiner.

[RESPONSE CONTINUES ON NEXT PAGE]